for use as reference lines are disposed under the semiconductor element and on the circuit forming surface. The adhesive lines adhere the semiconductor element to the circuit forming surface of the semiconductor substrate. The adhesive lines are respectively provided at positions corresponding to at least three corners of the semiconductor element.

This claimed configuration results in a semiconductor element that can be more accurately placed, and which can be more easily adhered to a semiconductor substrate. These and other advantages of the claimed invention are discussed in Applicant's specification on page 10, line 1, through page 12, line10. This claimed configuration is neither disclosed nor suggested by the cited reference.

Sono et al. disclose a semiconductor device 10 which comprises a multi-layer printed board 11, a supporting member 13, and a semiconductor chip 12 adhered to the supporting member 13 utilizing a die bonding material 23. This reference further discloses providing electrode parts 19 on a perimeter dent 18 formed in the multi-layer printed board 11. Additionally, this reference discloses that the supporting member 13 includes a die pad portion 21 and supporting bars 22. The supporting bars 22 are buried in the multi-layer printed board 11, with the die pad portion 21 being used for mounting the semiconductor chip 12.

However, and in contrast to the present invention, this reference does not disclose or otherwise suggest a plurality of adhesive lines which are adapted for use as reference lines, as recited by Applicant's independent claim 1. The Examiner's Action has noted that the cited reference does disclose die bonding material 23. However, this die bonding material 23 presumably has the same shape as the semiconductor chip 12,

and there is no disclosure or suggestion from this reference that the die bonding material 23 comprises a plurality of adhesive lines, as recited by Applicant's independent claim 1.

Furthermore, Applicant's independent claim 1 recites that the adhesive lines are disposed under the semiconductor element and on the circuit forming surface of the semiconductor substrate. The Examiner's Action has equated the container part 17 of the multi-layer printed board 11 and the dent 18 of the multi-layer printed board 11 as being a circuit forming surface. However, to the extent that the die bonding material 23 constitutes a plurality of adhesive lines, as recited in claim 1, this die bonding material 23 is not disposed on any feature of the multi-layer printed board 11, much less the features which the Examiner has equated as being a circuit forming surface, as would be required by Applicant's independent claim 1.

Furthermore, Applicant's independent claim 1 recites that the adhesive lines adhere the semiconductor element to the circuit forming surface of the semiconductor substrate. However, and in contrast, and to the extent that the die bonding material 23 constitutes a plurality of adhesive lines, it is noted that this die bonding material adheres the semiconductor chip 12 to the surface of the supporting member 3, instead of to a circuit forming surface of a semiconductor substrate, as would be required by Applicant's independent claim 1.

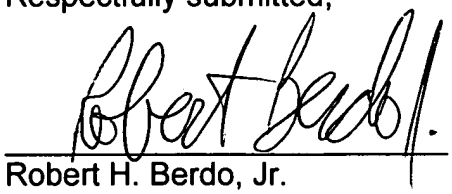
Furthermore, it is also noted that the Examiner's Action has equated the supporting bars 22, which form a component of the supporting member 13, as being reference lines. However, it is further noted that this reference specifically discloses that the supporting bars 22 are buried within the multi-layer printed board 11 (see

column 6, lines 38 - 40), so that even if these supporting bars 22 were adhesive, as would be required by Applicant's independent claim 1, they would not be in a position to adhere a semiconductor element to a circuit forming surface of a semiconductor substrate, as would be required by Applicant's independent claim 1. Moreover, since these supporting bars are disposed within the printed board 11, they could not serve as reference lines because they would not be viewable. As such, it is submitted that Applicant's independent claim 1 is *prima facie* patentably distinguishable over this reference. It is thus requested that this claim be allowed and it is further requested that this rejection be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



February 14, 2003
Date

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RHB:crh

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the following claim:

1. (Twice Amended) A semiconductor device, comprising:

a semiconductor substrate having a circuit forming surface, and having a plurality of electrode pads provided on the circuit forming surface, said electrode pads being disposed to surround an area of the circuit forming surface;

a semiconductor element mounted within the area of the circuit forming surface;

a plurality of adhesive lines adapted for use as reference lines [that include an adhesive], said adhesive [reference] lines being disposed under the semiconductor element and on the circuit forming surface, and being respectively provided at positions corresponding to at least three corners of the semiconductor element, said adhesive [reference] lines being adapted for use as a reference for determining a correct placement of the semiconductor element within the area of the circuit forming surface, said adhesive lines adhering said semiconductor element to the circuit forming surface of said semiconductor substrate; and

a sealing resin that seals said semiconductor element.